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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,790	09/26/2003	John Banning	TRAN-P243	9488

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WAGNER, MURABITO & HAO LLP  
Third Floor  
Two North Market Street  
San Jose, CA 95113

EXAMINER
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PAN, DANIEL H

ART UNIT	PAPER NUMBER
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2183

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/672,790	<b>Applicant(s)</b> BANNING ET AL.	
	<b>Examiner</b> Daniel Pan	<b>Art Unit</b> 2183	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03/20/07.
- 2a) ☐ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☐ Claim(s) \_\_\_\_\_ is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_\_ is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☒ Claim(s) 1-45 are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Election/Restrictions***

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-8, drawn to fetching from memory a first machine language instruction comprising an instruction segment; responsive to a trigger pattern in the first machine language instruction, modifying the instruction segment to form a second machine language instruction; and executing on the processor the second machine language instruction, classified in class 717, subclass 131.
- II. Claims 8-16, drawn to fetching from memory a first machine language instruction comprising an instruction segment; responsive to a trigger pattern in first machine language instruction, accessing instruction modification information from a memory; modifying the instruction segment according to the instruction modification information and information associated with said trigger pattern to form a second machine language instruction; and executing on said processor the second machine language instruction., classified in class 712, subclass 248.
- III. Claims 17-22, drawn to a computer system comprising:  
a memory for storing a first machine language instruction;  
a processor coupled to said memory for executing machine language instructions, implementing a fetching from the memory first machine language instruction comprising an instruction segment from the memory; responsive to a trigger pattern in first machine language instruction, modifying the instruction segment to form a second machine language instruction; and executing on the processor the second machine language instruction, classified in class 712, subclass 25.

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IV. Claims 23-32, drawn to a memory stored packet contained within a very long instruction word, comprising a trigger pattern to initiate modification of a segment of said very long instruction word, a first field to indicate the segment to be modified, and a second field to indicate how to modify a portion of the segment, classified in class 717, subclass 143.

V. Claims 33-36, drawn to accessing a machine language instruction from a memory, recognizing a trigger pattern in the machine language instruction, identifying a portion of the machine language instruction; and modifying the portion of the machine language instruction to a second machine language instruction, classified in class 711, subclass 215.

VI. Claims 37-45, drawn to accessing from memory an instruction word comprising a plurality of instruction segments and a trigger portion; based on trigger portion, identifying a portion of information of a memory queue for selection, based on trigger portion, identifying a portion of one of the plurality of instruction segments; modifying one of said plurality of instruction segments with the portion of information of the memory queue; and dispatching one of the plurality of instruction segments, as modified, to an execution unit of the processor, classified in class 710, subclass 54.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination I has separate utility such as a system which does not have the accessing instruction modification information from a

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memory responsive to the trigger pattern in the first machine language (II). See MPEP § 806.05(d).

Inventions I and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination I has separate utility such as a system which does not have which does not have the processor coupled to the memory for executing machine language instructions (III). See MPEP § 806.05(d).

Inventions I and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination I has separate utility such as a system which does not have the first field to indicate the segment to be modified, and a second field to indicate how to modify a portion of the segment (IV). See MPEP § 806.05(d).

Inventions I and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination I has separate utility such as a system which does not have the identifying a portion of the machine language instruction (V). See MPEP § 806.05(d).

Inventions I and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope

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and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination I has separate utility such as a system which does not have identifying a portion of information of a memory queue for selection and the dispatching one of the plurality of instruction segments, as modified, to an execution unit of the processor (VI). See MPEP § 806.05(d).

Inventions II and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination II has separate utility such as a system which does not have the processor coupled to the memory for executing machine language instructions and implement the method (III). See MPEP § 806.05(d).

Inventions II and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination II has separate utility such as a system which does not have the first field to indicate the segment to be modified, and a second field to indicate how to modify a portion of the segment (IV). See MPEP § 806.05(d).

Inventions II and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination II has separate utility such as a system which does not have the identifying a portion of the machine language instruction (V). See MPEP § 806.05(d).

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Inventions II and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination II has separate utility such as a system which does not have identifying a portion of information of a memory queue for selection and the dispatching one of the plurality of instruction segments, as modified, to an execution unit of the processor (VI). See MPEP § 806.05(d).

Inventions III and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination III has separate utility such as a system which does not have the first field to indicate the segment to be modified, and a second field to indicate how to modify a portion of the segment (IV). See MPEP § 806.05(d).

Inventions III and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination III has separate utility such as a system which does not have the identifying a portion of the machine language instruction (V). See MPEP § 806.05(d).

Inventions III and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is

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separately usable. In the instant case, subcombination III has separate utility such as a system which does not have identifying a portion of information of a memory queue for selection and the dispatching one of the plurality of instruction segments, as modified, to an execution unit of the processor (VI). See MPEP § 806.05(d).

Inventions IV and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination IV has separate utility such as a system which does not the identifying a portion of the machine language instruction (V). See MPEP § 806.05(d).

Inventions IV and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination IV has separate utility such as a system which does not have the identifying a portion of information of a memory queue for selection and the dispatching one of the plurality of instruction segments, as modified, to an execution unit of the processor (VI). See MPEP § 806.05(d).

Inventions V and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination IV has separate utility such as a system which does not have the identifying a portion of information of a memory queue for selection and the dispatching one of the plurality of instruction segments, as modified, to an execution unit of the processor (VI). See MPEP § 806.05(d).



The examiner has required restriction between subcombinations usable together. Where applicant elects a subcombination and claims thereto are subsequently found allowable, any claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions require a different field of search (see MPEP § 808.02). For example, search for Group I would not require search for the particular scope of accessing instruction modification information from a memory, which would require

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search for the access of the control storage of instruction modifications. Therefore, restriction for examination purposes as indicated is proper.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or invention to be examined even though the requirement be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention or species may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse.

Should applicant traverse on the ground that the inventions or species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions or species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C.103(a) of the other invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172.

The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

***21 Century Strategic Plan***

DANIEL H. PAN  
PRIMARY EXAMINER  
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